Virtual System Prototyping

1. Extraction
2. Virtual System
3. Virtual Compliance
Extraction

- Layout Geometry
- Broadband S-Parameters
  - Frequency Dependent
  - Causal/Passive
- SPICE Compliant Models
Layout Integration for Extraction

- Layout Generated in ECAD System
- AnsoftLinks
- HFSS
- Q3D Extractor
- 3D CAD Model
- Workbench
- Siwave
- Icepak
- Ansoft Designer
- Integrated HFSS Solver
- Stackup
- 3D View
3D Modeler Approach

To assign the same variable within HFSS

- Area select all objects above the layer UNNAMED_4
- Click Edit > Arrange > Move
- Define a Z only distance
- Go into Object tree and highlight all the objects that have a ‘Move’ in the history
- Click on the X,Y,Z coordinates in the Properties window
- Change the Z dimension to $diel_thickness
- Define $diel_thickness to a value
- Go to select ‘face’ mode
- Highlight the top of the dielectric material, and the tops of all the through hole vias
- Right click and select Edit > Surface > Move Faces > Along vector
- Define a Z only distance
- Go into Object tree and highlight the top dielectric object and the vias that have a ‘Move’ in the history
- Define a variable for ‘Move’
HFSS Solver On Demand – Advantages

- Layout Methodology
  - Layout, Stackup, and Padstack Editors
  - Parametric Design Environment
  - Automated Geometry Clipping
  - Maintain Trace Characteristics and Nets from Layout
- Port Setup
- Hierarchical Design – Chip/Package/Board
- Layout Optimized HFSS Settings
- Integrated Platform
PCB Layout

2D Layout View

Stackup Editor
Create PCB Ports

Select Trace Edges in Layout

Automatically create coupled waveports
Hierarchal Design - Package on PCB

Package layout is a sub-circuit of the board cutout.

Package stackup is independent of the PCB.

Package placement layer and position can be specified in the Footprint.
Merged Package and PCB Cutouts

2D Layout View

3D Layout View
Integrated Platform
HFSS Solver on Demand - Solve
Export to 3D HFSS Model from Designer

Integrate 3D Components with PCB/Package Designs
HFSS in Cadence Enables More Robust 3D Investigation

• Today, we will show the advances that we have made in our Solver on Demand capabilities which enable
  – The solving of larger 3D models to determine optimal performance
  – The ability to add and solve manufacturing variations to the 3D model
HFSS in Cadence – Automation and Ease of Use

- Select nets of interest
  - Signal, Power and Ground
- Draw extents to export selected portions of package or pcb
- Create ports on signal nets
- Specify HFSS solution setup
- Specify HFSS airbox extents
HFSS in Cadence
Package - Select Nets and Determine Extents
HFSS in Cadence
Package - Automatic Port Creation
HFSS in Cadence
Package - Airbox Extents and HFSS Solution Setup

Solution Frequency: 10 GHz

Adaptive Solution
Maximum Number of Passes: 10
Maximum Magnitude Delta S: 0.02

Solution Options
Order of Basis Functions: Mixed Order

Enable Iterative Solver
Relative Residual: 0.0001

Frequency Sweep
Type: Linear Step
Range: Start: 0.0 GHz, Stop: 20 GHz, Step: 0.01 GHz

Airbox Extents
Horizontal Padding: 0, Vertical: Pos: 0.2, Neg: 0.2

Export
Clip nets at extents

Host: localhost
Port: 2001 - 2002
Extraction

- Layout Geometry
- Broadband S-Parameters
  - Frequency Dependent
  - Causal/Passive
- SPICE Compliant Models
Differential Insertion and Return Loss

Insertion Loss

Return Loss
Frequency Dependent Materials

1. Multipole Debye Model Input
   - This lets you provide the measured data of relative permittivity and loss tangent versus frequency. Based on this data the software dynamically generates frequency dependent expressions for relative permittivity and loss tangent.

2. Djordjevic-Sarkar Method
   - HFSS allows you to enter the relative permittivity and loss tangent at a single measurement frequency. You may optionally enter the relative permittivity and conductivity at DC.
   - This is the best method if you don’t have measured data.
Causality Enforcement: Interpolating Sweeps

**Sweep 1**

- **Name:** Sweep 1

- **Type:** Interpolating
  - **Relative error for:** 0.5%
  - **Zo percent error:** 1%
  - **Enforce causality:** Enabled

**Specify frequency sweep**

- **Type:** Linear Step
- **Start:** 1 GHz
- **Stop:** 10 GHz
- **Step:** 0.1 GHz

**Sweep description:**

Linear Step from 1GHz to 10GHz, step=0.1GHz
Macro-modeling Functionality

New functionality for Designer 7

Network Data Explorer
- State-space fitting
- Passivity enforcement
- Passivity checker
- S-parameter visualization
- S-matrix reduction
- Macro-model generation

Circuit Simulation
- Designer
- Simplorer
- Other

Measured Data

HFSS

Q3D

SIwave

Other

Slwave

Design

• State-space
• Simplorer
• Spectre
• HSPICE
• PSPICE
Network Data Explorer

Differential Pairs

<table>
<thead>
<tr>
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<tbody>
<tr>
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<td></td>
<td>Diff1</td>
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<td>Comm1</td>
<td>25.00</td>
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<td>Diff5</td>
<td>100.00</td>
<td>Comm5</td>
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</table>
Network Data Explorer

- The S-Parameter data can be converted to a macro model for use with circuit simulation in multiple formats:

  - Original Option (fast but memory intensive).
  - New default, IFPV. Much lower memory requirements. Effective for high port counts.

Advanced features:

- Desired Fitting Error: 0.5 %
- Maximum Order: 400
- Convex optimization algorithm
- Iterated fitting of passivity violations
- One column at a time
- One entry at a time
- TWA
- Iterative rational function

New!
Virtual System Prototyping

1. Extraction
2. Virtual System
3. Virtual Compliance
AMI stands for Algorithmic Modeling Interface

It allows users to specify their own transmitter and receiver models as C-interface compiled libraries

- Designer supports Matlab as well as compiled DLLs
- Faster signal processing algorithms
- Intellectual property protection

Mainly used in convolution (fast) transient engines for channel simulation

- Designed to be used with fixed time step data

Introduced in IBIS 5.0 specs

- [http://eda.org/pub/ibis/ver5.0/ver5_0.txt](http://eda.org/pub/ibis/ver5.0/ver5_0.txt)
- IBIS stand for “I/O Buffer Information Specification”; high-level buffer specification for circuit modeling
- In these specs the library is specified inside the IBIS wrapper and the interface is called IBIS-AMI
New AMI Import Process

Import from .ibs file or specific .ami file directly
New AMI Import Process

- Automatically fill out fields for .dll and .so models
- Test button runs IBIS committee parser and reports pass/fail
- Advanced option used to set up models with non-standard behavior
Advanced Options Form (Optional)

- Model parameter tree
- Sample Parameters string
- Test results details
AMI model parameters can be sweep able component parameters upon import.

<table>
<thead>
<tr>
<th>Port</th>
<th>Value</th>
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<tbody>
<tr>
<td>Port1</td>
<td>R149</td>
</tr>
<tr>
<td>Port2</td>
<td>R150</td>
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<td>Port3</td>
<td>R151</td>
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<td>Port4</td>
<td>R152</td>
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<td>R153</td>
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<td>R154</td>
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<td>Port7</td>
<td>R155</td>
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<td>Port8</td>
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<td>Port10</td>
<td>R158</td>
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<tr>
<td>Port11</td>
<td>R159</td>
</tr>
<tr>
<td>Port12</td>
<td>R160</td>
</tr>
</tbody>
</table>

AMI Source
ID=26
AMI Probe
ID=32
Port1 Port2 Port3 Port4 Port5 Port6 Port7 Port8 Port9 Port10 Port11 Port12

AMI Source
ID=192

Tx
0

Rx
0
Pkg on PCB model from HFSS Solver on Demand

15 inches long stripline differential pair from Designer library

Makes use of GPU card
Eye Opening Before Receiver
Eye Opening After Receiver DFE
Part 1: Summary

• HFSS in Designer and Cadence enables SI engineers to setup and solve package and pcb models in 3D using HFSS

• Designer provides a complete framework to
  – Import ready to solve models from third party layout
  – Enables HFSS Solver on Demand to solve HFSS models
  – Check for passivity and causality to determine quality of S parameters and W elements
  – Enforce passivity and causality on S parameters and W elements
  – Greatly simplify the reading and execution of AMI models for transmitter and receivers through the new AMI importer
  – Validate channel performance with statistical eye diagrams and various eye measurements

• HFSS in Cadence (a Solver on Demand feature) greatly enhances productivity of an SI engineer
Automating The SI Design Flow For HFSS
Manufacturing Variations

- When you take the dimensions of the HFSS model to be fabricated, the ideal shape of the traces/pads/vias can become distorted because of the manufacturing process of etching copper.
- It is critical to simulate these manufacturing variations in order to validate your design will work after the manufacturing processes.
- This process has become automated.
HFSS Solver On Demand – Advantages

• Layout Methodology
  • Layout, Stackup, and Padstack Editors
  • *Parametric Design Environment*
  • *Automated Geometry Clipping*
  • *Maintain Trace Characteristics and Nets from Layout*

• *Port Setup*

• Hierarchical Design – Chip/Package/Board

• Layout Optimized HFSS Settings

• *Integrated Platform*
Assigning Variables

• Trace Width
Assigning Variables – Layout Approach

- Dielectric Thickness
Assigning Variables

- Etching Factor
Surface Roughness

- At high frequencies, currents follow small surface imperfections on conductor surfaces
  - Increases loss
- Mathematical models approximate loss increase due to surface roughness
  - Hammerstad
  - Groisse
  - Hemispherical
- These work well for modest levels of roughness, but tend to underpredict loss for very rough surfaces
- PCB manufacturing processes often process layers to make them rough in order to improve layer adhesion
Huray Model

- Huray Model treats a conductor surface as if it were stacked with small spheres
  - Approximates the effect of electrodepositing a surface layer of copper on a smooth copper foil for better adhesion
  - Assumes more surface area than Groisse model; can better model significantly rough surfaces
Huray Surface Roughness Model

- Improved surface roughness model for copper on laminates
Geometry Clipping

- Name the Partitions
- Automatically creates lumped ports at splits
- Automatically creates gap ports on pins (solderball/solderbumps)
- Automatically creates RLC Boundaries across the Capacitor pads
Divide and Conquer

• Why divide the model if we have the technology/hardware to solve it end-to-end?

• Smaller models enable quicker investigation of:
  • 3D Discontinuities
    – Ground return paths
    – Over/Under Etching
    – Stackup
    – Via Performance
High Performance Computing (HPC)

- HPC enables increased productivity and higher fidelity simulation - including more geometric detail and larger systems.
- Using HPC you can make your engineering staff, and your product development process, more productive and efficient. Faster turnaround and larger models all mean better designs in less time.
# HPC Capabilities

<table>
<thead>
<tr>
<th>High Performance Computing (HPC) License</th>
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<tbody>
<tr>
<td><strong>Domain Decomposition (DDM)</strong></td>
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<tr>
<td><strong>Multi-Processing</strong></td>
</tr>
<tr>
<td><strong>Distributed Solver Technology</strong></td>
</tr>
</tbody>
</table>

**Domain Decomposition (DDM)**
- Mesh Based
  - HFSS FEM
- Matrix Based
  - HFSS-IE
- Spectral
  - Frequency Sweep

**Multi-Processing**
- HFSS
- Designer
- Q3D Extractor
- Slwave
- Maxwell

**Distributed Solver Technology**
- HFSS
  - DDM with IE Domains
- HFSS-Transient
  - Distributed Excitations
- Q3DExtractor
  - DCRL, ACRL, CG
Spectral Domain Decomposition
Distributed Frequency Sweeps

### HFSS – BGA End

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<tr>
<th>#pts</th>
<th>Clock Time</th>
<th>Delta to Reference</th>
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<tr>
<td>Reference 301</td>
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<td>DSO Interpolating 301</td>
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### HFSS – Connector End

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<tr>
<td>Reference 301</td>
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<tr>
<td>DSO Interpolating 301</td>
<td>3h15m</td>
<td>10x</td>
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</table>
DSO Capabilities

Distributed Solve Option (DSO) License

Distributed Design Variations
(Optimetrics)

- HFSS
- Designer
- Q3D Extractor
- Simplorer
- Maxwell
### Design Variations – Study 8 Variations

**Distributed Solve**

<table>
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<th>Delta to Reference</th>
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<tr>
<td>DSO Variations</td>
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<td>13h</td>
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</table>

#### HFSS – BGA End

- **6x Faster**

#### HFSS – Connector End

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<tr>
<td>DSO Variations</td>
<td>8</td>
<td>11h</td>
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</tbody>
</table>
Hardware Utilization

- **Hardware**
  - 9 Dell R610 – 12 Cores, with 64GB RAM
  - Windows Server 2008 R2

- **Nodes**
  - 18 Nodes
    - 2 Frequencies or Variations per Machine
    - HPC for MP used to consume all cores on each Machine
Parametric W-Element Models

- Distributed Solve for 2D Transmission Lines
- Same variables used for the transmission lines
Parametric Variations for Virtual System

- Circuit Schematic for System
- A parametric sweep is used to characterize the system response to manufacturing variations
Parametric Sweep Results
DesignXplorer Integration

Ansoft Desktop

DSO

Solve

DesignXplorerer

Results

Design Points

Response Surface

Optimization

Sensitivity

Design for Six Sigma

Candidate Designs

Variable Sensitivity

Design for Manufacturing
Conclusion

- HFSS
  - Advanced Layout Capabilities
    - Improved Extraction
    - Enhanced Frequency Sweep techniques
    - New Broadband SPICE model generation

- Ansoft Designer
  - Advanced Simulation Technology
    - IBIS AMI
    - Full Channel for Compliance

- Productivity Enhancements
  - HPC for Speed
  - Distributed Solve for Design Space Characterization