Application Requirements

What do users want?
- Zero latency
- Infinite bandwidth
- Zero power
- Zero cost
- Infinite capacity
- Backward compatibility, future extensibility
- Programmable access granularity
- Absolute reliability

More realistic user expectations
- Better performance at lower cost
How to get “Better Performance”

- **Higher Capacity**
  - In-memory databases
    - more capability
  - OLTP databases
    - Less disk access, lower average latency
  - Consolidated (virtual) servers
    - More emulated servers in single system = lower response latency

- **Higher Bandwidth**
  - “Typical” scientific code
    - Higher throughput

- **Lower Latency**
  - single threaded code

- **Low Power**
  - Enables large capacity applications
  - Enables mobile/battery based applications
Memory System Selection Criteria

- No single answer defines “better performance”
  - Sometimes lower power, lower data rate, longer latency is “better performance”
  - Sometimes lower datarate, longer latency, higher capacity is “better performance”
  - Sometimes higher datarate, same latency, same capacity is “better performance”

- JEDEC member companies drive future specification requirement based on own respective application set

- Specification “frame” scaling decision for near future designs
Synchronous DRAM (SDRAM)

- Moved from signal interface to command interface
  - Enables programmable, pipelined operations
  - Consecutive data phases in single burst designed for CPU cacheline fill

- Multiple banks per device
  - Facilitates pipelining, different banks may be in different phases of row-cycle operation

- \{DDR3, GDDR5, LPDDR2\} - all direct evolutionary descendants of SDRAM
From SDRAM to DDR3

<table>
<thead>
<tr>
<th></th>
<th>SDRAM</th>
<th>DDR SDRAM</th>
<th>DDR2 SDRAM</th>
<th>DDR3 SDRAM</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate</td>
<td>66~133</td>
<td>200~400</td>
<td>400~1066</td>
<td>800~2133</td>
<td>MT/s</td>
</tr>
<tr>
<td>Voltage</td>
<td>3.3</td>
<td>2.5</td>
<td>1.8</td>
<td>1.5 (1.35)</td>
<td>V</td>
</tr>
<tr>
<td>Capacity</td>
<td>16~512</td>
<td>256~1024</td>
<td>256~2048</td>
<td>1024~4096</td>
<td>Mb</td>
</tr>
<tr>
<td>Burst length</td>
<td>1, 2, 4, 8</td>
<td>2, 4, 8</td>
<td>4, 8</td>
<td>4*, 8</td>
<td></td>
</tr>
<tr>
<td>I/O Type</td>
<td>LVTTL</td>
<td>SSTL-2</td>
<td>SSTL-18</td>
<td>SSTL-15</td>
<td></td>
</tr>
<tr>
<td>Termination</td>
<td>Off chip</td>
<td>Off chip</td>
<td>On die</td>
<td>On die</td>
<td></td>
</tr>
<tr>
<td>Dynamic ODT</td>
<td>N/A</td>
<td>N/A</td>
<td>No</td>
<td>RttWR</td>
<td></td>
</tr>
<tr>
<td>Bank count</td>
<td>2*, 4</td>
<td>4</td>
<td>4, 8*</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>I/O Calibration</td>
<td>None</td>
<td>None</td>
<td>OCD*</td>
<td>ZQ</td>
<td></td>
</tr>
</tbody>
</table>

- Small evolutionary steps to increase data rate, lower voltage and add features
## Memory (System) Access Latency

### Component Access Latency
- Commodity DRAM (DDR3)
  - Open page ~13 ns
  - Close page ~26 ns
- NAND Flash
  - ~25,000 ns

### System Access Latency Example
- "DRAM" only responsible for ~30% of ~100 ns of "memory access latency"
- TLB misses, buffering/re-drive, FIFO, serial-to-parallel, parallel-to-serial conversions, etc. all increase latency
Commodity DRAM Latency Scaling Trend
Commodity DRAM Datarate Scaling Trend
Key Challenges
1. Transmitter
2. Transmission Line
3. Receiver
4. Terminator
5. Clocks

- Taken from “Signaling in High-Performance Memory Systems,” John Poulton, *ISSCC Tutorial, 1999.*
Channel Topology

- Multiple DIMMs per channel
- 2 ranks (loads) per DIMM
- Dynamic ODT
- Asymmetric R/W topology
## Current Typical System Memory Configuration

<table>
<thead>
<tr>
<th>Supply voltage</th>
<th>Loading / Speed</th>
<th>800-1066</th>
<th>1333</th>
<th>1600</th>
<th>1866</th>
<th>2133</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DR</td>
<td>QR</td>
<td>DR</td>
<td>QR</td>
<td>DR</td>
<td>QR</td>
</tr>
<tr>
<td>1.5V</td>
<td>1DPC</td>
<td>✔️</td>
<td>✔️</td>
<td>✔️</td>
<td>✔️</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>2DPC</td>
<td>✔️</td>
<td>✔️</td>
<td>✔️</td>
<td>-</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>3DPC</td>
<td>✔️</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1.35V</td>
<td>1DPC</td>
<td>✔️</td>
<td>✔️</td>
<td>✔️</td>
<td>✔️</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>2DPC</td>
<td>✔️</td>
<td>✔️</td>
<td>✔️</td>
<td>-</td>
<td>✔️</td>
</tr>
<tr>
<td></td>
<td>3DPC</td>
<td>✔️</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1.25V</td>
<td>1DPC</td>
<td>✔️</td>
<td>✔️</td>
<td>✔️</td>
<td>✔️</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>2DPC</td>
<td>✔️</td>
<td>✔️</td>
<td>✔️</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>3DPC</td>
<td>✔️</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Looking Forward
LRDIMM 4Rx4

- **Density:** 16G
- **Target platform:**
  - Westmere
  - Romley
  - Interlagos
- **Compatible with DDR3 DIMMs**
- **20% cost advantage over equivalent LRDIMM**
Best candidate to replace/augment DRAM?
  — Flash

Why?
  — It’s cheaper than DRAM

Both DRAM and Flash running into process scaling challenges
  — Alternative technologies making claims and trying to win mindshare
  — DRAM and Flash are multi-billion dollar industries with continuous re-investment

Revolution postponed until
  — Effectiveness of billion dollar investments in DRAM/Flash loses to million dollar investments in alternatives.
High Level Goals for DDR4

- **Latency**
  - Comparable or slightly lower than DDR3

- **Bandwidth**
  - Data rate to 3.2 Gb/s and beyond

- **Power**
  - Lower power by lowering voltage AND new features to suppress idle and active power

- **Cost**
  - Minimize additional die size penalty relative to DDR3

- **Capacity**
  - Leverage TSV to create extreme-capacity systems

- **Compatibility**
  - Leverage as much infrastructure from DDR3 as practicable
DDR4 Features
(Subject to Change)

- **Pseudo Open Drain, faster I/O**
  - Leveraged from GDDR5

- **Single-ended signaling**
  - Continues on DDRx legacy, may be end of line

- **1:1 signal/ground ratio**
  - Better noise shielding on connector for higher data rate

- **Higher data rate, lower voltages**

- **Smaller rows for x4 device**
  - X4 devices to have lower activation power and better performance

- **Same prefetch length as DDR3**
  - Supports existing CPU cache infrastructure

- **GDDR5-style bank groups**
  - High data rate, low DRAM core cycle rate, same prefetch length
**Basic idea: Same register device for both RDIMM and LRDIMM**

- DDR4 Register + DRAM + no data buffers = RDIMM
- DDR4 Register + DRAM + data buffers = LRDIMM
Through Silicon Via (TSV)

- (Potentially) a real revolution in DRAM technology
  - Within DRAM generation event horizon, 3~5 years

- Can enable direct attach memory to processor
  - Low power, low latency
  - May have slightly higher per bit cost structure

- Mitigate the bandwidth-vs-capacity issue
  - Multiple DRAM dies in single stack presents single electrical {address, data} load to system
DRAM Stacks with TSV

- **Traditional Dual Die Package (DDP)**
  - Same DRAM die as used in single die packages
  - System sees all loads on all DRAM dies

- **DRAM with TSV**
  - Special die for TSV use
  - System sees single load of separate I/O re-drive chip
TSV Benefits and Drawbacks

**Benefits**
- Can be used as (In-package) direct attach memory
- Mitigates capacity-vs-bandwidth trade-off
- Enables ultra-high capacity memory systems not possible today

**Drawbacks**
- Increased cost basis for DRAM manufacturers
- Different dies used for SDP and stacked devices
- Require new manufacturing/testing models for direct attach memory function between different devices from different companies