Thermo-Mechanical Modeling of TSVs

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Introduction to Through-Silicon Vias (TSVs)
Advantages of TSVs over wire bonding in packages
Role of TSVs in addressing thermal issues in packages
Case study of stacked die package
  • Thermal modeling of 3D Package with and without TSVs
    – TSVs modeled as lumped and detailed
  • Structural Modeling of 3D Package with TSV’s
    – Thermo-Mechanical modeling of TSV’s
Conclusions on modeling TSV based on results from simulations
Introduction to TSVs

Through-Silicon Vias (TSVs) are an emerging technology to address 3D integration of dies in a package.

TSVs are vertical structures in that pass through lower chips as a direct interconnect to chips above:

- Eliminates the need for wire bonds
- Implements complex, multi-chip systems entirely in silicon
- Combines the best aspects of system-on-chip (SOC) and system-in-package (SIP) scheme
Hardware

Samsung Announces Stacked DRAM Chips Using Through-Silicon Via

Marcus Yam (Bloomberg) - April 24, 2007 12:56 PM

Samsung Electronics steps up chip stacking with memory packages that are faster, smaller and consume less power.

Samsung Electronics has released details on its own all-DRAM stacked memory package using through-silicon via (TSV) technology. The new wafer-level processed stacked package (WSP) consists of four 512Mb DDR2 DRAM chips that offer a combined 2Gb of high-density memory. Using the TSV-processed 2Gb DRAMs, Samsung says it can create a 4Gb DIMM based on advanced WSP technology, while reducing overall package size, power use and increasing chip speed.

In today’s MCUs, memory chips are connected by wire bonding, requiring vertical stacking and increasing overall chip size. According to Samsung, TSV technology eliminates these issues, allowing closer chip packing and reducing power consumption.

In 2010, Samsung Electronics, Samsung Electronics, and Samsung Electronics announced plans to mass produce TSV memory chips. TSV technology has the potential to revolutionize the semiconductor industry by allowing for higher chip density and more efficient chip design.

Intel to unveil new way to connect chips

By Michael Kanellos and Stephen Shankland
Staff Writers, CNET News

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SAN FRANCISCO-Intel on Thursday will unveil a way to open the data paths between chips, a move that could help overcome a huge hurdle in increasing processor performance, CNET News.com has learned.

Called through-silicon via (TSV), the technique involves stacking chips vertically in a package and then creating connections between the bottom of the top chip and the top of the bottom chip. These wires will greatly expand the means to exchange data between chips, sources said.

In 2001, Intel Capital, the chipmaker's venture arm, invested in a company that has a TSV application.

Semiconductor process expert Tera-Si Technologies, based in Sunnyvale, Calif., demonstrates how the technology works in this slide show.

Justin Rattner, a senior fellow at Intel who helps set the company's technology agenda, will discuss TSV in a speech on Thursday at the Intel Developer Forum.

Fast chips, and new dual- and multicore chips, have in turn created a problem around getting data to and from the different pieces of silicon inside a PC.

Several companies are proposing solutions to the problem. Sonics Microsystems, for instance, is promoting proximity communications. In this technique, overlapping chips communicate with special patches separated by a thin air gap.

Intel is also working on ways to allow faster communication between the cores in its dual-core chips, said Steve Smith, vice president in the company's Digital Enterprise Group.

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Advantages of TSVs Over Wire Bonding in Packages

Structural Advantage

• Eliminates the need for wire bonds allowing for space saving
  – In extremely compact chips (mobile devices, etc.) wire bonds would limit the number of stacked chips due to increasing length
  – With TSVs, the packages are only limited by the chip sizes themselves

Process Time Advantage

• The distance information must travel on a chip can be upwards of 1000 times smaller
  – There are now direct, straight paths rather than much longer multi-directional wire bonds
Role of TSVs in Addressing Thermal Issues in Packages

As chip powers increase and their size decreases, there is a much larger chance of overheating.

Stacked chips increase the need for thermal management by increasing the total power load in the package.

TSVs are a combination of copper pillars and vias that directly connect the chips and play an important role in that heat transfer:

- Higher thermal conductivity than surrounding silicon
- Direct (shorter) path than wire bonds for less resistance
A flip chip stacked die package typically used in mobile devices is considered.

Analysis is carried out in ANSYS Icepak comparing a model with and without TSVs:

- Silicon die vs. Lumped conduction TSVs
- Lumped conduction TSVs vs. Detailed TSVs
  - In system-level or very detailed TSV models it is difficult to model TSVs in detail
    - Scale of TSVs 1/100 of the die

Maximum temperatures are monitored and temperature distribution is viewed to compare results.
Geometry & Boundary Conditions Considerations

TSV Chip-1: Logic Chip- 8.5x8.5x0.1mm
Chip-2 Memory Chip 6.5x6.5x0.1mm
Substrate- 13.5mm x13.5mm x 1 mm
Micro Bumps (Copper)-Dia-0.20 mm, Height- 0.1mm
TSV Columns- Dia-0.025 mm, Pitch 0.2 mm

Convective b.c.
(h=10w/m² k)
Lumped Conductivity Approximations

Arrived Lumped conductivity
• 183.6 Normal (Through-Plane)
• 182.8 In-Plane (Can just use the default silicon property as well)

In the 8.5 mm x 8.5 mm silicon die there are 1764 TSV’s of 25 μm diameter

Overall area ratio 1.2% (Through-Plane)

Material Conductivities
• Silicon - 181.15 W/mK
• Copper - 387.6 W/mK
Meshing Disparities

Meshing

- Even with a relatively fine mesh, the mesh count for ¼ symmetry on the lumped conduction model is 30,856
- Because of the fine detail of the vias, the ¼ symmetry mesh is 1,198,486
  - Lumped pillars between chips
Case: 1 Temperature with and without TSV

Die Properties Adjusted to Include TSVs (Lumped Conduction)

Note: Using symmetry considerations 1/4\textsuperscript{th} of Package is modeled
Temperature contours with and without details of TSV

Die Properties Adjusted to Include TSVs (Lumped Conduction)

Actual TSVs modeled
Zoomed View of Temperature Distribution
Thermo-Structural Analysis of 3D Package with TSV
Need for Thermo-Structural Analysis

Induced stresses affects transistor performance by the piezo-resistant effects

Transistor performance may get affected by TSVs which are close

• High stresses result from coefficient of thermal expansion (CTE) mismatch between copper and silicon

3-D integration requires evaluation of thermo-structural stresses which in turn effect the performance of transistors in proximity
Case Study (Thermo-Structural)

A flip chip stacked die package typical in mobile devices considered for Thermo-Structural

The package configuration is similar to the one considered for thermal analysis

It is essential to add vital components like Cu-pads and simplify the model for structural simulation

5x5 array of TSV is considered in the inner core near the hot spot region

Cu-pads are modeled on top and bottom of TSV’s for holding the TSV

Analysis is carried out in ANSYS Mechanical by transferring thermal results to structural simulation by Workbench transfer utility

Maximum Equivalent stress, thermal strains are monitored at critical locations
Material Properties & Case Settings

Standard Material Properties available in Literature are used in current study

CTE (Copper)- 1.8E-05/°C

Temperature dependent CTE used for Silicon

Orthotropic CTE is used for both Substrate and PCB

Bottom face of the PCB is fixed and automatic contacts are used in Mechanical
Workbench Project Schematic for Thermo-Structural Simulation
Results
Temperature Comparison in Icepak and Structural

Icepak

Structural
Temperature Comparison in Icepak and Structural (TSV Region)
Equivalent Stress (TSV Chip)
Thermal Strain (TSV & Cu-Pads)
Observations and Conclusions

Maximum temperature is not being greatly effected by TSV
• This is due to TSV sitting in a high conductivity material (silicon in current study). This may change if the die conductivity varies
• This is due to the overall % of TSV in the silicon which is under 5%. This may change if the overall % of TSV increases

Lumped approximation works for TSVs in silicon with relatively low TSV area %
• This would be recommended for thermal-only system-level modeling
Observations and Conclusions

It has been observed that high Temperature in the TSV region causes thermal strain that may affect performance of close by transistor

It has been observed that the maximum equivalent stress occurs between TSV and silicon because of CTE mismatch

While increased number of TSVs or diameter of TSVs may begin decreasing temperature, the designer would need to watch for adverse effects from increased thermal stresses
Thank You

Questions?