Ansoft Designer Analysis for High-Speed Serial Interconnects

Greg Pitner
Problem Statement

- SI engineers use simulation software to squeeze the most performance out of their design.
- They will tend to focus on via transitions, escape routing from BGA or connectors, or even the transitions from package to board or board to connector.
- These optimal design dimensions are then used to create the entire board/package.
Problem Statement

• When you take the dimensions of the HFSS model to be fabricated, the ideal shape of the traces/pads/vias can become distorted because of the manufacturing process of etching copper

• It is critical to simulate these manufacturing variations in order to validate your design will work after the manufacturing processes

• This process has become automated
Agenda

- Show how manufacturing variations can be included in 3D simulations
- Show how Distributed Solve Option (DSO) enables users to obtain design variation solutions dramatically faster than running serially
ANSYS Simulation Approaches

• In 2006, we were helping customers like NXP, Tessera, and Amkor design the optimal dimensions for optimal performance.
Also in 2006, companies like Intel and Molex were aware of the problems of manufacturing variations to fabricated designs. They were interested in using our tools to model these variations for a SATA System.
ANSYS Simulation Approaches

- In 2010, we showed how we can use DesignXplorer in conjunction with DesignerSI to investigate surface responses of a channel design with parametric variations.

**PCle Channel Example**

12 components consisting of multiple design parameters varying from material specific to physical.
Defining Manufacturing Variations with HFSS Accuracy

- Identify partitions
- Automatically creates lumped ports at splits
- Automatically creates gap ports on pins (solderball/solderbumps)
- Automatically creates RLC Boundaries across the Capacitor pads

Cadence

DesignerSI Layout
Divide and Conquer

• Why continue to divide the model if we have the technology/hardware to solve it end-to-end?

• Smaller models enable quicker investigation of:
  • Anti-pads geometry
  • Stackup
  • Manufacturing tolerances
  • Etc...
Assigning Variables – Layout Approach

- **Dielectric Thickness**

```
<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Material</th>
<th>Thickness</th>
<th>Etch</th>
<th>Lower</th>
<th>Separation</th>
</tr>
</thead>
<tbody>
<tr>
<td>top_ref_plane</td>
<td>signal</td>
<td>copper</td>
<td>0mil</td>
<td></td>
<td>101.9mil</td>
<td></td>
</tr>
<tr>
<td>UNAMED_0</td>
<td>dielectric</td>
<td>AIR</td>
<td>20mil</td>
<td></td>
<td>81.9mil</td>
<td>17.8mil</td>
</tr>
<tr>
<td>TOP</td>
<td>signal</td>
<td>COPPER</td>
<td>2.2mil</td>
<td></td>
<td>81.9mil</td>
<td></td>
</tr>
<tr>
<td>UNAMED_2</td>
<td>dielectric</td>
<td>FR-4</td>
<td>3.6mil</td>
<td></td>
<td>78.3mil</td>
<td>3mil</td>
</tr>
<tr>
<td>02_GND1</td>
<td>signal</td>
<td>COPPER</td>
<td>0.6mil</td>
<td></td>
<td>78.3mil</td>
<td></td>
</tr>
<tr>
<td>UNAMED_4</td>
<td>dielectric</td>
<td>FR-4</td>
<td>$diel_thickness</td>
<td>74.2mil</td>
<td>3.5mil</td>
<td></td>
</tr>
<tr>
<td>03_SIG1</td>
<td>signal</td>
<td>COPPER</td>
<td>0.6mil</td>
<td></td>
<td>74.2mil</td>
<td></td>
</tr>
</tbody>
</table>
```

Options:
- Use the simplified auto-align editing mode.

```
Treat as infinite ground for Planar EM analysis
```

HFSS Etch Factor: 0

Total stackup height: 2.58826mm
Assigning variables – 3D Modeler Approach

To assign the same variable within HFSS:

- Area select all objects above the layer UNNAMED_4
- Click Edit > Arrange > Move
- Define a Z only distance
- Go into Object tree and highlight all the objects that have a ‘Move’ in the history
- Click on the X,Y,Z coordinates in the Properties window
- Change the Z dimension to $\text{diel\_thickness}$
- Define $\text{diel\_thickness}$ to a value
- Go to select ‘face’ mode
- Highlight the top of the dielectric material, and the tops of all the through hole vias
- Right click and select Edit > Surface > Move Faces > Along vector
- Define a Z only distance
- Go into Object tree and highlight the top dielectric object and the vias that have a ‘Move’ in the history
- Define a variable for ‘Move’
Assigning Variables

- Trace Width
Assigning Variables

• Etching Factor
Surface Roughness

- At high frequencies, currents follow small surface imperfections on conductor surfaces
  - Increases loss

- Mathematical models approximate loss increase due to surface roughness
  - Hammerstad
  - Groisse
  - Hemispherical

- These work well for modest levels of roughness, but tend to underpredict loss for very rough surfaces

- PCB manufacturing processes often process layers to make them rough in order to improve layer adhesion
Huray Model

• Huray Model treats a conductor surface as if it were stacked with small spheres
  • Approximates the effect of electrodepositing a surface layer of copper on a smooth copper foil for better adhesion
  • Assumes more surface area than Groisse model; can better model significantly rough surfaces
Huray Surface Roughness Model

- Improved surface roughness model for copper on laminates
Passivity Enforcement: Interpolating Sweeps

- Additional criteria to determine convergence
- Passivity violations used as new basis points
- Improves reliability of models in transient SPICE simulations
Frequency Dependant Materials

1. Multipole Debye Model Input
   - This lets you provide the measured data of relative permittivity and loss tangent versus frequency. Based on this data the software dynamically generates frequency dependent expressions for relative permittivity and loss tangent.

2. Djordjevic-Sarkar Method
   - HFSS allows you to enter the relative permittivity and loss tangent at a single measurement frequency. You may optionally enter the relative permittivity and conductivity at DC.
   - This is the best method if you don’t have measured data.
Distributed Solve Option (DSO)

Problem is subdivided, and each subproblem is solved on a separate machine (including the Local Machine)

Available distributions
- Parametric variable sweeps
- Frequency sweeps (HFSS)

- Same distributed analysis license works for Designer (Planar EM), ePhysics, HFSS, Maxwell, and Q3D Extractor
Configuring the Machines

- Swept 8 variations from the 3 variables assigned to the models
- DSO using 9 Windows Server 2008 machines with 12 cores and 64 GB RAM each.
- Used 6 MP for each machine to have a total of 18 machines for the Frequency Sweep
- Used 6MP for Parametric Sweep
## DSO Solution Times – BGA End

### Frequency Sweep
- Nominal Project using DSO for the Frequency Sweep
- Adaptive Passes
  - 55 mins
- Frequency Sweep
  - 1 hour 46 mins
- WITHOUT DSO
  - 16 hours 30 mins

### Parametric Variations
- Solved 8 variations from the 3 variables available
- Cumulative Solve Time
  - 82 hours 11 mins
- Longest Solve Time
  - 12 hours 48 mins
- Time Savings
  - **6.4X**
DSO Solution Times – Connector End

**Frequency Sweep**

- Nominal Project using DSO for the Frequency Sweep
- Adaptive Passes
  - 49 mins
- Frequency Sweep
  - 3 hours 15 mins
- WITHOUT DSO
  - 34 hours

**Parametric Variations**

- Solved 8 variations from the 3 variables available
- Cumulative Solve Time
  - 82 hours 43 mins
- Longest Solve Time
  - 11 hours 9 mins
- Time Savings
  - 7.4X
Using DSO with 2D Extractor for Long Transmission Lines

• For long uniform transmission lines, it is best to use a 2D field solution
• Same variables used for the transmission lines
Schematic Setup for Parametric Variations

- The 3 models are stitched together in schematic
- A parametric sweep is created that controls all 3 models
Parametric Sweep Results

XY Plot 4

Circuit 1

Curve Info

- $dB(S(\text{Port1,Port1}))$
- Linear Frequency
- $brd\_trace\_width=3.2\, \text{mil} \quad diel\_thickness=3.6\, \text{mil} \quad trace\_etch=0$
- $dB(S(\text{Port1,Port1}))$
- Linear Frequency
- $brd\_trace\_width=4\, \text{mil} \quad diel\_thickness=3.6\, \text{mil} \quad trace\_etch=0$
- $dB(S(\text{Port1,Port1}))$
- Linear Frequency
- $brd\_trace\_width=3.2\, \text{mil} \quad diel\_thickness=4.6\, \text{mil} \quad trace\_etch=0$
- $dB(S(\text{Port1,Port1}))$
- Linear Frequency
- $brd\_trace\_width=4\, \text{mil} \quad diel\_thickness=4.6\, \text{mil} \quad trace\_etch=0$
- $dB(S(\text{Port1,Port1}))$
- Linear Frequency
- $brd\_trace\_width=3.2\, \text{mil} \quad diel\_thickness=3.6\, \text{mil} \quad trace\_etch=3$
- $dB(S(\text{Port1,Port1}))$
- Linear Frequency
- $brd\_trace\_width=4\, \text{mil} \quad diel\_thickness=3.6\, \text{mil} \quad trace\_etch=3$
- $dB(S(\text{Port1,Port1}))$
- Linear Frequency
- $brd\_trace\_width=3.2\, \text{mil} \quad diel\_thickness=4.6\, \text{mil} \quad trace\_etch=3$
- $dB(S(\text{Port1,Port1}))$
- Linear Frequency
- $brd\_trace\_width=4\, \text{mil} \quad diel\_thickness=4.6\, \text{mil} \quad trace\_etch=3$
- $dB(S(\text{Port1,Port1}))$
- Linear Frequency
- $brd\_trace\_width=3.2\, \text{mil} \quad diel\_thickness=3.6\, \text{mil} \quad trace\_etch=0$
- $dB(S(\text{Port1,Port3}))$
- Linear Frequency
- $brd\_trace\_width=4\, \text{mil} \quad diel\_thickness=3.6\, \text{mil} \quad trace\_etch=0$
- $dB(S(\text{Port1,Port3}))$
- Linear Frequency
- $brd\_trace\_width=3.2\, \text{mil} \quad diel\_thickness=4.6\, \text{mil} \quad trace\_etch=3$
- $dB(S(\text{Port1,Port3}))$
Conclusion

• We showed how Solver on Demand enables easier translation and merging of complex geometries
• We showed how manufacturing variations can be captured in the 3D model
• We showed the power of DSO to speed up parametric sweeps