Signal-, Power-Integrity, & EMI Update

Bill McGinn
Senior Application Engineer
Overview

- ANSYS ECAD Solutions
- HFSS for Signal Integrity
- SIwave Full BRD and PKG Solutions
- SI Circuit Simulation for IBIS-AMI and Memory
- Q3D Extractor 11.0 Updates
ANSYS ECAD Solutions

Fluid Dynamics  Structural Mechanics  Electromagnetics  Systems and Multiphysics
AnsoftLinks Translation Paths

- Cadence
- Mentor
- ODB++
- Altium
- Zuken

Static ECAD Transfer (.anf)

- TPA
- Q3D
- Slwave
- HFSS
- Designer
- Icepak
- Mechanical

Dynamic ECAD Transfer

AnsoftLinks with Extracta

- Cadence
  - Virtuoso
  - SiP
  - APD
  - Allegro

Solver on Demand

- HFSS
- PlanarEM
- Nexxim
- HSPICE
HFSS for Signal Integrity

ECAD & Field Solver Improvements
Problem Description:

1. Converting package and printed circuit board layout data to 3D mechanical CAD models creates a large amount of unnecessary overhead in the geometry database.

2. A key capability needed for wide-spread use of HFSS as an extraction tool is to make it accessible to non experts.

Solution:

1. When HFSS is used for package and PCB extraction a 2D Electrical CAD layout editor is better suited for model creation and setup.

2. The Designer Layout editor with Solver on Demand improves HFSS accessibility for non-expert engineers who need to use HFSS for package and PCB extraction.
   - It provides an EMI solution for 2 layer pkg and board design with HFSS and PlanarEM.

3. The Designer Layout editor with Solver on Demand significantly reduces the engineering time required to set up package and pcb models for extraction with HFSS.

4. Cadence design flows allows a user to solve with HFSS from within the Cadence environment using Cadence Extracta and an IPC link.
“HFSS for ECAD”

Two Design Flows for Electrical Design
• Mechanical CAD
  – Connectors, Waveguides
  – HFSS
• Electric CAD (layout)
  – PCBs, Packages, On-chip Passives
  – HFSS - Solver on Demand
HFSS Setup & Solve Within Cadence SPB

- Dynamic ECAD Flow
- Create and Solve models with HFSS from within Cadence Allegro, APD, & SiP
HFSS Setup & Solve Within Virtuoso

- Setup & Solve
- Lumped ports
  - Horizontal & Vertical
- Layer Stack Up Simplified
- Automated Via Clustering
- Back Annotation of Touchstone

Back annotation scheduled for final release
HFSS Package & PCB Merge

Independent package and board stackups

Copy package

Paste into PCB layout

Project Manager

pkg_mgtt

fga4448_6vlx240t_ff1156_120508

transrapid_SI_new

Definitions

Synchronize Design

Make copy
Design is copied, same stackup as parent, manufacturable with parent

New design
fga4448_6vlx240t_ff1156_120508

No copy - use instance of original
Design is linked to original, unrelated stackups, not manufacturable with parent

Package

Board

HFSS - Solver on Demand
Parameterized Padstacks

Enables parametric investigation of via geometry, or optimization.

Applied to global padstack definition. Therefore, project variables are used:

<table>
<thead>
<tr>
<th>Padstack</th>
<th>Pad</th>
<th>Anti pad</th>
<th>Thermal pad</th>
<th>Connect pt</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>circle (19mil)</td>
<td>circle ({$d1})</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>Default</td>
<td>circle (19mil)</td>
<td>circle ({$d1})</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>GND-2</td>
<td>circle (19mil)</td>
<td>circle ({$d1})</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>SIG-3</td>
<td>circle (19mil)</td>
<td>circle ({$d1})</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>VCC-4</td>
<td>circle (19mil)</td>
<td>circle ({$d1})</td>
<td>none</td>
<td>none</td>
</tr>
</tbody>
</table>

Pad settings:
- Shape: Circle
- Diameter: 19mil
- Offset X: 0mil
- Offset Y: 0mil

Anti pad settings:
- Shape: Circle
- Diameter: {$d1}
- Offset X: 0mil
- Offset Y: 0mil

Thermal pad settings:
- Shape: None
- Offset X: 0mil
- Offset Y: 0mil

Connection point settings:
- Direction: none

Add layer
Remove layer
Parameterized Differential Vias
HFSS Port Assignment by Pad

Select pad -> RT Click -> Create Port

Port name is derived from pad name
HFSS ECAD Layout Editor

- Tag differential nets for s-parameter postprocessing.

- Turn net visibility on/off.
Huray Surface Roughness: Modeled vs. Measured

HFSS ECAD Layout Editor

Parameterizable Etch Factor

Automatic Causal Djordjevic Sarkar Dielectric Models

Parameterizable Surface Roughness
Passivity Enforcement: Interpolating Sweeps

Additional criteria to determine convergence
Passivity violations used as new basis points
Improves reliability of models in transient SPICE simulations
Lump Port De-embedding (Calibration)

Physical dimensions of lump port carries current

• “intrinsic inductance”

Analytic inductance is de-embedded from port S-parameters

“Calibrating” the “test fixture” of the measurement

Implementation analogous to wave port de-embedding
HFSS ECAD – Causal Sweep Option

Option to fit an interpolation sweep with causal basis functions

Very efficient fitting and guarantees causal S-parameters

ANSYS Causality Checker
- 1.8 % error without causal enforcement
- 0.0 % error with causal enforcement
HFSS for the SI Community Summary

New in R14

- Parameterized padstacks
- Automated causal material
- Multi-frequency point adapting
- Integrated 2D/3D views
- Huray Surface Roughness Models
- Lumped Port De-embedding
- Trapezoidal Trace Cross-sections
- Automated Virtuoso HFSS Design
- Passivity Enforced Interpolation

- HFSS Solves from within Cadence
Show Nets in HFSS for MCAD

“Show Nets” identifies 3D conducting paths between terminals
SIwave Full BRD and PKG Solutions

DDR3 and High Speed Serial Serial Improvements
Memory and High Speed Serial Improvements

Solver

Signal Net Analyzer
• Ideal and non-ideal lumped parameters (i.e. Zo)
• Nexxim and HSPICE RLC simulations

Via to Via Coupling
• Differential pair accuracy improvements

Solver Support for Arbitrary Antipad Cutouts
• Improvement in via modeling accuracy

SYZ Solver Improvements
• Guaranteed passive/causal SYZ solutions

FWS Improvements for Large Port Count Devices
• Faster convergence and reduced RAM when using “Iterated Fitting of Passivity” for large port count devices

Improved “Push Excitation” Accuracy & Robustness
• SIwave now forces required interpolation from Designer 7.0.

Improved Surface Roughness
• Added Huray surface roughness model

PI Advisor Improvements
• Genetic Algorithm supports weighting of constraints
• Genetic Algorithm supports new constraints
  – Maximum Total Capacitor Area
  – Maximum Number of Capacitor Types

Improved SYZ Storage Architecture
• 6x reduction in disk space for SYZ parameters

GUI

64 bit GUI for Windows

Table Impedance Calculator
• Flight time plots
• Transient Simulations with Nexxim or HSPICE

PKG & PCB Automation
• Graphical selection & merging

Pin Grouping Automation
• Multi-part select with group per part/net definitions

Improved Validation Checker
• Detection of pins belonging to multiple pin groups

Automated DCIR Reports

Equipotential Pads for DCIR Solver

Temperature Profile Plotting from Icepak

Improved Surface Roughness
• Addition of Huray model in GUI

PI Advisor Improvements
• Allowance of weighting constraints in GUI
• Additional constraints added
  – Maximum Total Capacitor Area
  – Maximum Number of Capacitor Types

Improved ODB++ Support

Support for X2Y Low Inductance Capacitors
DDR3 Solutions: Signal Net Analyzer

- Displays $Z_0$, length, time delay, and reference layer
- All possible paths (from each pin to every other pin on net) are displayed – Sorted in descending order of path distance
- User can click on an individual path in the table – Variation in $Z_0$ is graphically displayed – Path is highlighted in SIwave’s main layout window
- Ideal reference layer mode (default) – Traces on top & bottom metal layers are assumed to be microstrips – Interior traces are assumed to be striplines
- Non-ideal reference layer mode – Reference layer is explicitly calculated for each trace segment – Some traces may be floating (no suitable reference layer available)
Automated DCIR Reporting
SI Circuit Simulation for High Speed Serial and Memory Applications
Macromodeling Functionality

New functionality for the SI market

Network Data Explorer
- State-space fitting
- Passivity enforcement
- Passivity checker
- S-parameter visualization
- S-matrix reduction
- Macro-model generation

Measured Data

Circuit Simulation
- Designer
- Simplorer
- Other

State Space
- Simplorer
- Spectre
- HSPICE
- PSPICE

HFSS
Q3D
SIwave
Designer
Macro-Modeling with Network Data Explorer

Touchstone Models from Arbitrary Source can be converted to Multiple Model Types with Causality and Passivity Enforcement!

Advanced features
Design Engineers require accurate electrical models for components when designing circuits. A key feature of the web-based library support is ease of use. Library installation generally requires users to download files, uncompress them, and place them in the correct location on a local drive. Automated web-based download from within Designer automates these steps, making it easy for users to keep their component libraries up to date.

Design Kits
- DDR3, PCIe 3.0, HDMI, SATA, SAS, …

Scripting Libraries
- FWS commands, Footprinting, Reporting Templates, …
High Speed Serial Design with IBIS-AMI

- Automated IBIS-AMI Importing
  - IBIS-AMI Specification Testing
    - Pass/Fail
    - Advanced
User Defined Transmit Jitter for HSS Design

PDF vs. time defined in a text file userdefined.txt

Contents of text file userdefined.txt:

<table>
<thead>
<tr>
<th>Value</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2e-12</td>
<td>.1</td>
</tr>
<tr>
<td>6e-12</td>
<td>.5</td>
</tr>
<tr>
<td>1e-11</td>
<td>1.0</td>
</tr>
<tr>
<td>1.2e-11</td>
<td>.5</td>
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<tr>
<td>1.9e-11</td>
<td>.1</td>
</tr>
<tr>
<td>2e-11</td>
<td>0</td>
</tr>
</tbody>
</table>
Q3D Extractor 11.0
Q3D Extractor Overview

Major Applications
- 64 Bit Windows GUI
- Magnetic Materials
- Terminal Setup Improvements for AC RL Solver
- Touch Panel Expression Caching for CG and RL
- Selectable Frequency Export for Lumped SPICE Passives
- DCRL Speed Up
- CG Convergence improvements
- HPC Improvements
  - Network Installs
  - Fixed Variables
    - Greatly improves post processing speed for projects with large numbers of variables
      - i.e. Via Wizard
- 3D Modeling Enhancements
- WB Integration Improvements for DSO & Optimetrics
Touch Screen Accuracy Improvements

- Added the ability to converge on off diagonal terms with Touch Panel displays
Q3D – Magnetic Materials

Simulation Time

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>Maxwell 3D</th>
<th>50 min</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q3D AC</td>
<td>10 s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q3D DC</td>
<td>6 min 30 s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sweep</td>
<td>2 s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>&lt; 7 min</td>
<td></td>
<td>50 min</td>
</tr>
<tr>
<td>Peak RAM</td>
<td>0.6 GB</td>
<td></td>
<td>5 GB</td>
</tr>
</tbody>
</table>

Electroplated Nickel has $\mu \cong 5$

Bulk Nickel has $\mu \cong 600$

*Each additional frequency point takes ~15 minutes to solve with Maxwell
3D Modeler Enhancements

View customization.

- Z-stretch.
- 64-bit user interface
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