RFID Radio Circuit Design in CMOS
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ABSTRACT

This paper describes a reference design with circuits and an antenna for a UHF RFID system. A new Class 2 (Gen 2) tag was designed, including the extremely low-power integrated circuit integrated with an inexpensive printed antenna. Details on the design of the rectifier power regulator, demodulator, reset circuit, modulator, and antenna are highlighted. The paper includes a system-level software verification of the RFID tag system to determine proper voltage regulation and signal demodulation.

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INTRODUCTION

Radio Frequency Identification (RFID) is an electronic tagging technology that allows an object, place, or person to be automatically identified at a distance without a direct line-of-sight using a radio wave exchange. Applications include inventory tracking, prescription medication tracking and authentication, secure automobile keys, and access control for secure facilities. RFID is a major trend that provides fundamental shifts along several business vectors and is expected to be a major growth area in wireless electronics. Details of RFID applications and opportunities can be found in many previously published works [1-3].

This paper details a specific design of a passive backscatter UHF RFID tag circuit that meets the requirements set forth in the EPCglobal Class-1, Generation-2 Protocol [4]. EPCglobal is an organization dedicated to the worldwide adoption and standardization of RFID technology. The design specification sets forth all physical and logical requirements for the tag air interface and digital state machine design.

The first section of this paper gives an overview of the RFID system followed by a section that discusses the tag design criteria for predicting range based on the tag integrated circuit power consumption. Issues limiting range, especially the channel electromagnetic effects, are highlighted. Analog circuit design for a 900 MHz tag is the subject of the next section, with specific circuit design and results for the rectifier, regulator, reset circuit, demodulator and modulator circuit. Antenna design and simulation of a simple meander-line dipole tag antenna is performed. The paper concludes with a system-level simulation that includes all of the circuit blocks to predict DC power generation and reader-to-tag and tag-to-reader communication.

Figure 1. UHF RFID System Diagram
RFID SYSTEM OVERVIEW

In a Class-1, Generation-2 protocol system, a reader transmits information to a tag by modulating an RF signal in the 860 – 960 MHz frequency range. The tag receives both information and operating energy from this RF signal. Tags are passive, meaning that they receive all of their operating energy from the reader’s RF transmission. If the transponder lies within the range of the reader, an alternating RF voltage is induced on the transponder antenna and is rectified in order to provide a DC supply voltage for tag operation.

The reader receives information from a tag by transmitting a continuous-wave (CW) RF signal to the tag. The tag responds by modulating the impedance placed on the antenna terminals, thereby backscattering an information signal to the reader. Figure 1 is a system diagram illustrating the RFID reader, tag and backscattering mechanism. The reader sends information to one or more tags by modulating an RF carrier using double-sideband amplitude shift keying (DSB-ASK), single-sideband amplitude shift keying (SSB-ASK) or phase-reversal amplitude shift keying (PR-ASK) at a bit rate ranging between 26.7 to 128 Kbits/s. Modulation is achieved using a pulse-interval encoding (PIE) format wherein data is passed to the tag by pulsing the carrier wave at differing time intervals to indicate a 0 or 1 bit.

Tags only respond after they receive commands from the reader, and there is a rigorous protocol for allowing a single reader to manage many tags during an inventory session. The EPCglobal specification provides all details of the protocol for tag selection, identification (singulation), and anti-collision. Once a command has been sent, the reader emits a CW signal to continuously provide power to the tags. The selected tag then backscatters energy by commutating the impedance that is applied to the input to the tag antenna. Figure 1 illustrates the mechanism schematically in the diagram of the tag modulator, which selectively places one of two impedances across the antenna terminals as commanded by the digital logic block (a low-power digital state machine). The tag can use either ASK or phase shift keying (PSK) modulation at a bit rate ranging between 40 to 640 kbits/s for FM0 baseband encoding or 5 to 320 kbits/s for Miller sub-carrier encoding.

TAG DESIGN CRITERIA

The goal for the design of a modern gen-2 tag is to maximize read range while providing full compliance with the protocol. Read range is primarily limited by the forward link from the reader to the tag. The tag is entirely passive and relies on the energy provided by the incident radiation to power up. It must receive sufficient energy for all tag circuits during an inventory session. Indeed, the tag circuitry has a minimum threshold below which no communication can proceed. The power received by the tag diminishes quadratically with distance; hence, tags in close proximity to the reader are far more likely to have sufficient power for operation compared to tags farther away. A modern UHF tag, such as the Atmel ATA5590 [5], has a read range of 10 meters and a total power consumption of less than 12µWatts.
POWER AND RANGE

The available power received by the tag is governed by the Range Equation [6]. The fundamental power relationship between the transmitter and the receiver of any communication system begins with consideration of an isotropic radiation source. An isotropic source emits power equally in all directions. The power density on a hypothetical sphere of radius \( r \) can be calculated by dividing the transmitted power by the area of that sphere:

\[
p(r) = \frac{P_t}{4\pi r^2} \text{ Watts/m}^2
\]

Equation (1) is the power density that will be seen by the tag antenna when the reader and tag are separated by a distance \( r \). Of course, the tag antenna intercepts only a portion of the transmitted power depending upon the effective area of that antenna \( A_e \). The received power, therefore, is given by

\[
P_r = p(r)A_e = \frac{P_t A_e}{4\pi r^2} \text{ Watts.} \tag{2}
\]

Equation (2) gives the maximum power available at the tag given an isotropic radiator and an effective area of the tag antenna. The FCC almost always specifies limits on radiation based on an Effective Isotropic Radiated Power (EIRP). In North America, for example, the EIRP limit for UHF RFID is 4 Watts. The transmitted power \( P_t \) in equation (2) can be replaced by the EIRP:

\[
P_r = \text{EIRP} \frac{A_e}{4\pi r^2} \text{ Watts.} \tag{3}
\]

The relationship between the tag antenna gain \( G_r \) and the tag antenna effective area \( A_e \) is

\[
G_r = \frac{4\pi A_e}{\lambda^2} \tag{4}
\]

where \( \lambda = \frac{c}{f} \) is the free space wavelength, \( c \) is the speed of light, and \( f \) is the operating frequency. Replacing \( A_e \) in (3) using (4) allows us to come to a final expression for the available power at the tag due to a given transmit EIRP

\[
P_r = \frac{\text{EIRP} \cdot G_r \lambda^2}{(4\pi r)^2} \text{ Watts.} \tag{5}
\]

As will be discussed in more detail later, a tag antenna is often a variation of a dipole. A classic half-wave (length = \( \lambda/2 \)) dipole has a gain \( G = 1.64 \). Using EIRP = 4W, \( G_r = 1.64 \), \( r = 10 \) meters, and \( f = 950 \) MHz in equation (5) results in a receive power \( P_r = 41.4 \) \( \mu \)Watts. Clearly, the tag design must be extremely low power to operate on micro Watts.

ISSUES LIMITING RANGE

Now equation (5) really only indicates the available power to the tag antenna. The actual power accepted by the tag circuit could be significantly less, depending upon several loss mechanisms, including antenna mismatch, polarization mismatch, antenna misalignment, and environmental scattering. Any number of loss mechanisms can be added to (5) by multiplying by loss factors that range from 0 to 1. For example, we can include a polarization loss factor \( p \), where \( 0 \leq p \leq 1 \) and an antenna mismatch factor \( \tau \) where \( 0 \leq \tau \leq 1 \) in equation (5) to take into account these loss mechanisms [7]

\[
P_r = \frac{\text{EIRP} \cdot G_r \lambda^2 \cdot p \cdot \tau}{(4\pi r)^2} \text{ Watts}. \tag{6}
\]

As was shown in [7], the mismatch factor \( \tau \) is given by

\[
\tau = \frac{R_c \cdot R_a}{|Z_c + Z_a|^2} \tag{7}
\]

where \( Z_c = R_c + jX_c \) is the input impedance to the tag chip and \( Z_a = R_a + jX_a \) is the tag antenna impedance.

These equations can be used to compute the power available at the antenna terminals given the transmit EIRP and the range. As mentioned earlier, the tag can only begin operation once the input power has exceeded a certain threshold \( P_{th} \). Rearranging (6) allows us to compute the range \( r \) in terms of the other parameters including the threshold power:

\[
r = \frac{\lambda}{4\pi} \sqrt{\frac{P_r}{PEIRP \cdot G_r \cdot \tau \cdot p}} \text{ meters.} \tag{8}
\]

For example, using the previous values plus a chip threshold power \( P_{th} = 10 \) \( \mu \)Watts, and a mismatch factor of 0.5 and polarization loss factor of 0.5 yields a range \( r = 10 \) meters.
**ANALOG CIRCUIT DESIGN AND PERFORMANCE**

Figure 2 is a block diagram of a typical UHF RFID tag. The system is divided into two main sections, viz., the analog front end and the digital state machine.

The analog front end performs all analog processing for DC power, receive signal detection/demodulation, and transmit modulation. The digital state machine decodes incoming data, responds to commands from the transmitter (reader), reads and writes to internal EEPROM memory, and encodes and transmits data to the modulator. The analog front end has several internal analog sub-blocks. The rectifier converts RF energy received by the antenna into DC power for all other blocks. The regulator is followed by a voltage regulator that limits and regulates voltage produced by the rectifier. The reset sub-block provides a reset signal indicating that the rectified voltage has reached a reliable, regulated level. The envelope detector detects and demodulates the reader data signal and produces the digital demodulated signal. A ring oscillator generates the clock for the digital state machine. The modulator places the modulated signal onto the tag antenna by alternating the load impedance on the antenna terminals.

In the remainder of this section, we discuss the design of the analog front end circuits in a low-power UHF RFID tag. All circuits were designed using the TSMC 0.18µm standard CMOS process.

**RECTIFIER**

The rectifier block uses a cascaded Dickson voltage multiplier circuit with multiple cascaded sections in order to convert the extremely low input voltage up to a potential sufficient for operating CMOS circuits. For our design, we used a 4-stage charge pump using diode-connected minimum length PMOS transistors as rectifiers. The bulk terminals of the PMOS transistors were tied to the gate and drain terminals (back-bias) to reduce the effective threshold voltage. The transistor size and the value of the MIM capacitors were optimized using harmonic balance simulations. Figure 3 shows the rectifier circuit.

*Figure 2. UHF RFID tag block diagram depicting the analog front-end and digital state machine.*
Voltage regulation is accomplished by using a voltage limiter followed by a regulator circuit. The limiter circuit shown in Figure 4 ensures the input voltage level to the voltage regulator is below the transistor breakdown voltage of 3.3V.

The linear voltage regulator circuit is shown in Figure 5. The voltage is regulated by taking the feedback signal to compare with a reference voltage in an error amplifier, and then the output of the amplifier can be used as a controlled signal to change the resistance of a pass-transistor. Figure 5 shows the circuit of voltage regulator which includes the startup and self-biased circuit on the left, bandgap reference circuit in the middle, and the voltage regulator as mentioned previously on the right. The output voltage level of the regulator is set to 1.25V, which will be the power supply voltage level for the digital circuits and the other analog circuits. Simulations revealed that the quiescent current consumption of the regulator is less than 200nA.
**RESET**

When the generated supply voltage from the charge-pump circuit is high enough, the reset signal should go to a “low” state to initiate state machine in the digital circuitry. To avoid false triggering, the circuit has to provide a hysteresis characteristic, which is achieved by turning on and off the circuit branch composed of M8 and M9 in Figure 6 when the “avdd” voltage is positively or negatively swept, respectively. Figure 7 shows the test input and output waveforms on the left of the figure, which can be re-drawn as the curve tracer plot as shown on the right such that the depth of hysteresis can be clearly seen.

![Figure 5. Linear voltage regulator circuit.](image)

![Figure 6. Reset circuit.](image)
DEMODULATOR AND RING OSCILLATOR

The demodulation circuit and the ring oscillator are shown in Figure 8. The two circuits share a bias circuit.

The demodulator is composed of a fast charge pump, a peak detector, and a comparator. The fast charge pump detects the ASK modulated RF signal envelope, which is further processed by the peak detector formed by a diode-connected MOSFET and capacitor to obtain its slow moving average. The envelope signal and its slowing moving part are then compared to produce the demodulated signal in digital format. The comparator circuit shown in Figure 9 is designed for rail-to-rail common mode input range to accommodate a wide tag operation range. Its hysteresis input-output characteristic also enables it to work under a noisy environment. Typical waveforms of the demodulation signals are shown in Figure 10.

The ring oscillator acts as the clock generator for the tag IC. Its design follows a paper by Sundaresan, et al. [8]. Its nominal oscillation frequency is 4 MHz and is designed to be insensitive to both process and temperature variations.

Figure 7. Reset circuit produces a reset signal once regulated voltage exceeds threshold.
Figure 8. Demodulator circuit detects incoming data.

Figure 9. Comparator circuit used for demodulation.
MODULATOR

The modulator modifies the capacitance of a varactor connected to the antenna according to the digital signal input. Varying the capacitance varies the radar cross section (RCS) of the antenna. The reader detects these variations so that the back-scattered information can be recovered on the reader side. Figure 11 shows the modulator circuit. The varactor is connected to the antenna terminals thru blocking capacitor. The voltage across the varactor is controlled by current biased inverted in the middle of the figure, which can slow down the speed of capacitance change such that the back-scattered modulated signal can meet the requirement of FCC emission regulation.

Figure 10. Demodulator output for ideal input data.

Figure 11. Modulator circuit.
ANTENNA DESIGN AND PERFORMANCE

The input impedance looking in to the rectifier circuit is primarily capacitive. The antenna must be matched to this capacitive input to maximize the power absorbed by the rectifier from the incident wave. It would be possible to use lumped reactive elements to create a matching circuit such as an L match to transform the capacitive input impedance to a pure real impedance for presentation to the antenna. Because of the cost sensitivity, however, it is impractical to use lumped elements hence it is desirable to implement the impedance matching in the antenna itself. Figure 12 depicts a meander-line dipole antenna that has a highly inductive input impedance [7]. The design also includes a loading bar that can be used to fine tune the resistance. The goal of the antenna design is to adjust the dimensions of the antenna such that the reactance of the antenna resonates with the reactance of the chip input impedance.

Figure 13 is a plot of the input impedance of tag’s front-end simulated with Nexxim®’s harmonic balance engine under large signal conditions with source impedance puling. As can be seen in the figure, the optimal source impedance for power transferred into the tag circuit is \( Z_s = 35 + j155 \, \Omega \) at 900 MHz, which is also the desired input impedance when performing antenna design. The antenna of Figure 12 was simulated using the planar method of moments electromagnetic field solver in Ansoft Designer®. Optimization was applied with a goal to achieve an input impedance of \( Z_i \) such that the maximum power can be transferred from the source (or antenna). In the initial design the optimizer reduced the inductance of the antenna by reducing dimension b and additionally attempted to push the loading bar as far away from the rest of the antenna. Values of \( L = 77.7 \, \text{mm}, \ b = 7 \, \text{mm}, \) and \( s = 5 \, \text{mm} \) resulted in an input impedance of \( Z_a = 12.5 + j148 \, \Omega \). It was decided to reduce the number of meanders and simultaneously remove entirely the loading bar. The final optimized design appears in Figure 14. The optimized dimensions are \( L = 121 \, \text{mm}, \ b = 2.85 \, \text{mm} \) resulting in an input impedance of \( Z_a = 34.3 + j155 \, \Omega \).

Figure 12. Meander-line inductive dipole antenna geometry before optimization.
Figure 13. Source impedance pulling result shows the optimal source impedance for maximum power transferring at $35 + j155 \Omega$ at 900 MHz.

Figure 14. Final design has just small meander sections to provide the inductive reactance to resonate with the rectifier input impedance. Final parameter values are $L = 121\, \text{mm}$, $b = 2.85\, \text{mm}$, and $Z_a = 34.3 + j155 \, \Omega$.

A frequency sweep electromagnetic simulation was performed to ensure that the antenna provides reliable performance across the UHF RFID band. Figure 15 is a plot of the input impedance versus frequency for the antenna in Figure 14. The antenna design provides relatively flat response across the entire UHF RFID band.

Figure 16 contains plots of the far-field radiation pattern of the antenna as computed by planar electromagnetic field simulation. The antenna exhibits a broad omnidirectional pattern with a gain of 1.95dB.
Figure 15. Swept frequency performance of the antenna in Figure 14 as computed by electromagnetic simulation.

Figure 16. Far-field pattern as computed by electromagnetic field simulation. The antenna exhibits a broad omnidirectional pattern with a 1.95 dB gain.
After all of the necessary circuits have been designed, it is worthwhile to put all of the blocks together in the system simulator to perform communication link analysis in simulation. The system bench for link test will include two portions. The first is reader-to-tag (i.e., uplink test) which is shown in Figure 17. The second is tag-to-reader (i.e., downlink test), which is shown in Figure 18. The reader is implemented using behavioral models in both cases. For tag-to-reader testing, the behavioral PSK demodulator on the reader side is also included to recover the PSK back-scattered modulated signal.
Figure 19. The Nexxim circuit detail in the previous figure, which includes one HFSS™
dynamic link component and one Nexxim netlist subcircuit described in Spectre® format.

Figure 20. The Cadence schematic representation for the Nexxim netlist subcircuit in Figure 20.
The EPCglobal protocol provides a long CW burst to allow tag power-up prior to sending data. The following simulation results show the power up behavior during that period of leading CW radiation. The supply voltage ripple can be observed under the condition of deep AM modulation. The recovered PIE waveform is shown in green in Figure 21.

Figure 22 shows back-modulated data as input on the tag side. As mentioned earlier, the back-scattered energy is experienced by the reader thru an RCS change. The data recovery can be seen on the reader side, although it is little bit noisy. The recovered timing and pulse period is well correlated to the input of modulated signal.
**SUMMARY**

In this paper we discussed the design and simulation of a UHF RFID tag and system that complies with the EPC-global, Class-1, Generation-2 specification. It was found that circuit performance on par with modern commercial RFID tag chips was achieved using the TSMC 0.18µm CMOS process. Designs and simulations for the analog front end of the tag including the rectifier, voltage regulator, reset, demodulator, and modulator circuits were illustrated. The paper included an antenna design that provides conjugate match with the input impedance of the rectifier. The paper closed with a top-level verification that combines behavioral modeling, HFSS antenna system modeling, plus Nexxim transient simulation, showing that the design provides reliable DC power and demodulated signals for both uplink and downlink.

**REFERENCES**
