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Applications such as WLAN, Bluetooth®, 3G, Gigabit Ethernet, and portable communications devices are fueling the demand for advanced Mixed Signal/RFCMOS semiconductors. Requirements for lower cost, lighter weight and longer battery life drive greater functional integration leading to sophisticated single-chip solutions. Modern portable consumer electronic systems, for example, combine high digital content for advanced user experience with high analog and radio frequency (RF) resources for connectivity to remote systems and services. This results in complex System on Chip (SoC) solutions that combine mixed-signal circuits, embedded high-performance analog and sensitive RF front-end blocks together with complex digital circuitry on the same chip.

UMC delivers advanced SoC solutions that address the needs of communications and networking industries for high-performance and low power digital and analog circuits. UMC has paid particular attention to the sensitive analog and RF circuits that are critical to the success of an IC design project. Addressing the analog section of the system with rigor can eliminate costly re-spins. To ensure high yield, the analog blocks must be as robust as the digital blocks and must take into account analog nonlinearities, parametric yield and process variations. Complexities in achieving this robustness force design organizations to search for new technologies and methods to deliver solutions that are rigorous and reliable. Of critical importance is the design flow and modeling for custom integrated circuits that include RF circuits on the analog front-end, analog and mixed-signal circuits at baseband, and digital signal processing on the back-end.

UMC and Ansoft have teamed to develop a design solution for complex systems that include custom RF and analog circuits. UMC’s advanced RFCMOS process combined with electronic design automation (EDA) tools from Ansoft and other established vendors provide the platform upon which advanced RFICs can be developed. Advanced simulation technologies provided by Ansoft’s Nexxim® simulator and HFSS™ 3D electromagnetic extractor enhance the Cadence RFIC design flow.

This joint effort leverages UMC’s production-proven 0.13um RFCMOS process with advanced circuit simulation and electromagnetic extraction tools from Ansoft. This document describes RF and analog design and verification in the RFIC design flow. Circuits from an on-going project to develop an ultrawideband (UWB) multi-band orthogonal frequency division multiplexed (MB-OFDM) radio will be used as the vehicle to demonstrate the process technology, EDA tools and design flow.
RFIC DESIGN CHALLENGE

RFIC designers face several significant challenges. Large RFICs, such as wireless transceivers, contain analog and digital components including voltage-controlled oscillators (VCOs), phase locked loops (PLLs), mixers, filters, amplifiers, automatic gain control (AGC) loops, digital-to-analog converters (DACs), and analog-to-digital converters (ADCs). Characterizing these elements requires detailed simulation in the time- and frequency-domains. In addition, simulating multiple radio elements cascaded to form a complete transceiver chain often exceeds the limits of traditional EDA tools. Too often designers are forced to compromise on the breadth of their verification simulations due to long simulation run time and short design schedules. New technology is needed to provide the accuracy and robust convergence required for sensitive analog blocks and the capacity and speed necessary for handling the large numbers of transistors and parasitic elements typical in mixed-signal SoC designs.

Modern radio systems operate at GHz frequencies under advanced signaling methods like orthogonal frequency division multiplexing (OFDM) and fast frequency hopping to maximize link reliability and minimize interference with other services. Circuits that perform at high frequency with high switching speed are extremely sensitive to active and passive device models, distributed layout parasitics, substrate coupling effects, inter-stage impedances, IC packaging, and power supply noise. Providing new methods that accurately characterize layout and other parasitic effects is more critical than ever to first pass success.

RFIC design requires specialized and unique analysis techniques specific to RF design. Nonlinear effects of harmonic distortion, gain compression, oscillator phase noise, and mixer noise figure are most often simulated and reported in the frequency domain. Switching behavior, circuit initial start-up, and transceiver response to instantaneous events such as frequency hopping are best examined in the time domain. Technology to allow simulation in the time- and frequency-domains with consistent results between is required for modern RF circuit simulation and verification.

Integrated circuits are eventually assembled into an IC package. In many cases, RF circuits are added to large SoCs in a single-chip solution. Another approach is to integrate RF circuitry by using system-in-package (SiP) techniques leading to similar verification challenges as found in SoC solutions. The most comprehensive system approach allows for a multi-die package that may include a digital SoC together with wireless, sensor and actuator die as necessary.

New technologies for circuit simulation capacity and speed that add value to a ready established flow can be integrated into existing design solutions. For analog and RF circuits, the most popular flow is the Cadence Virtuoso® Analog Design Environment (ADE). Ansoft’s products for advanced circuit and electromagnetic simulation are linked into that environment. Many RFICs contain the analog-to-digital converter (ADC), digital-to-analog converter (DAC), phase-lock loop (PLL), and possibly a digital synthesizer. These functions are generally created through a different environment and integrated on-chip. Verification of these blocks is still performed using SPICE-level circuit simulators for critical accuracy. The addition of Nexxim® new technology for high-performance circuit simulation combined with the reliability of the High-Frequency Structure Simulator (HFSS™) component and layout electromagnetic extraction into the design flow creates new opportunities for SoC designers to achieve first-pass silicon success.
Figure 1. RFIC Design and Verification Flow.
Figure 1 is a flow chart depicting the typical RFIC flow and Figure 2 is a functional chart that indicates tools used in that flow. The process begins with system design and behavioral modeling test bench development. Common modeling approaches are to use Matlab®, a high-level language like C, a hardware description language (HDL) like Verilog-A or VHDL-AMS, or dedicated system simulators like the one found in Ansoft Designer®. These tools are effective in creating a behavioral simulation of a system that may contain RF, analog, and digital sections. Figure 3 depicts a behavioral block diagram of a wireless system with blocks displaying the baseband digital signal processing (DSP), data converters, radio transmitter and receiver, and the radio channel. Behavioral models for each of these blocks can be created using the aforementioned tools. The level of detail in each behavioral model depends upon the requirements of the analysis and the maturity of the project. By modeling the full chip within a top-level test bench, verification of critical system performance in terms of constellation plots and metrics such as error-vector magnitude (EVM) or bit-error rate (BER) can be performed. Circuit block specifications are developed to define such metrics as gain, return loss, noise figure, sensitivity, effective number of bits (ENOB) for the data converters, etc.

This behavioral test bench ultimately serves as the framework for more complex mixed level simulations, where blocks can be inserted at the transistor level and verified in a system context. This allows designers to make a tradeoff between analysis rigor and simulation speed by inserting critical blocks at the transistor level and well-characterized blocks at the behavioral level. Continuous verification of system performance as blocks mature can be performed to track system evolution during the design process. Problems can be detected and mitigated early in the design cycle allowing corrective measures to be performed. Block design by disparate design teams can occur concurrently and assembled into the top-level simulation as they become available.
The behavioral modeling tool used for the UWB project is Ansoft Designer. It provides very comprehensive models for radio blocks such as mixers, filters, amplifiers, radio channel models, and antennas. Ansoft Designer also provides DSP and mixed-signal blocks often encountered in modern radio systems such as fast Fourier transforms (FFTs), data converters, symbol mappers, random bit sources, and detectors. A very significant advantage of this solution is that it can co-simulate with Matlab models and allows customization of user-defined blocks using standard C programming. For this RFIC project, Ansoft and UMC created a custom library of behavioral components for the UWB baseband signal processing including data scrambling, convolutional encoding, puncturing, symbol mapping and OFDM symbol generation. These models represent a Multiband OFDM Alliance1 (MBOA)-compliant system library that is available to UMC and Ansoft customers.

The next step in the flow is circuit design using idealized interconnect and foundry design kit device models. Circuits at this level are used for early design trades to select designs that meet performance specifications. Circuit simulation is performed in the time- and frequency-domains to characterize critical performance metrics. The choice of domain depends on the circuit, type of simulation, and desired output. The Nexxim® circuit simulator performs time-domain simulation with an optimized transient simulation engine; it performs frequency-domain simulation using a high-performance harmonic balance engine. UMC has been a leader in the adoption of this new and powerful technology. The Nexxim simulator is fully integrated into the Cadence RFIC design flow. Figure 4 illustrates the tight integration directly within the menu structure of Cadence ADE.

The value of transient plus harmonic balance in a single simulator is made apparent by time- and frequency-domain simulations on RF circuits. Figure 5 is the schematic for the UWB receiver analog baseband including the baseband filter and variable gain amplifier for automatic gain control (AGC). Peripheral elements surrounding the core circuit represent the circuit test bench that provides in-phase (I) and quadrature (Q) inputs and outputs and various control and power supply voltages. This circuit is designed using the UMC 0.13um Foundry Design Kit (FDK) models and simulations were performed using Ansoft’s Nexxim circuit simulator. Figure 6 provides typical frequency-domain results for this circuit including swept frequency results using linear network analysis, harmonic distortion results using Nexxim harmonic balance analysis, and gain compression. Figure 7 provides typical time-domain results for the same circuit including the input waveform for a complex OFDM input and the output I and Q channel responses for a single UWB frame using Nexxim transient simulation. A single process design kit and associated environment enables a smooth determination and selection of the simulation algorithm desired. Results are presented through a display appropriate for the selected simulation type. As circuits are completed at block level, they are verified within the top-level context with behavioral stimulus and descriptions for the surrounding chip.

1 The Multiband OFDM Alliance is a special interest group organized to develop, publish, and promote the best overall solution for global UWB standardization. See http://www.multibandofdm.org/ for more information.
Figure 4. Ansoft’s Nexxim circuit simulator is fully integrated into Cadence ADE.

Figure 5. Analog baseband of UWB receiver including baseband filter and variable gain AGC amplifier.
Figure 6. Example frequency-domain results for the baseband circuit in Figure 5. (a) Swept frequency response for various gain states, (b) Harmonic distortion as reported by harmonic balance simulation, and (c) Gain compression plot as computed by harmonic balance.

Figure 7. Example time-domain results for the baseband circuit in Figure 5. (a) OFDM digitally modulated input waveform using PWL source, (b) I and Q output as predicted by Nexxim.
RFIC DESIGN AND VERIFICATION

To improve the fidelity of the simulation, on-chip passive elements like spiral inductors and metal-oxide-metal (MoM) capacitors can be synthesized, extracted, and added to the circuit simulations. The foundry design kit passive models are highly accurate so long as design rules are followed and parameter ranges are not exceeded. UMC has provided a novel mechanism for device topologies outside those provided in standard design kits to enhance designer’s innovation. UMC’s Electromagnetic Design Methodology (EMDM) uses full-wave 3D simulation to create models for the on-chip passives with accuracy traceable to the foundry process. For spiral inductors, the inductance and quality factor (Q) is computed by Ansoft’s HFSS™ using advanced full-wave finite element simulation.

To simplify the process of using full 3D EM for circuit designers, UMC and Ansoft collaborated on the EMDM project. Ansoft created a tool called the Component Wizard for UMC to develop parameterized models that match their foundry design process. Figure 8 depicts the Component Wizard and the process used by UMC to create ready-to-solve parametric HFSS projects. The wizard uses the Cadence layout P-cell and layer stackup technology file to create HFSS projects. A library of fully parameterized spiral inductor geometries in HFSS has been produced using this method. The library is available to UMC customers as a foundry-validated EMDM design kit. The kit contains fully parameterized HFSS projects for spiral geometries including circular, rectangular, octagonal, and symmetric inductors. A methodology to back annotate the optimized design to common layout tools was also provided. Figure 9 provides plots that compare HFSS simulated results with measured results for two circular spiral geometries. As can be seen in the figures, agreement is excellent for both inductance and quality factor.

Figure 8. Component Wizard reads UMC process technology file and P-cells to create ready-to-solve parametric HFSS projects.
The next step in the process is to perform circuit layout. Automated design-rule-driven and connectivity-driven layout may be used judiciously, especially to take advantage of direct ties to schematic and design-rule-checking (DRC). Critical analog blocks, however, are generally manually routed using a full custom approach to ensure that highly sensitive analog circuitry meet specifications.

As layouts are completed, electromagnetic simulation is used to provide highly accurate models for interaction of passive components and interconnect. For example, several spiral inductors may be selected as highly critical and a target for EM simulation in a single project. These EM simulation models can replace the models that were created earlier in the design process, and can be mixed and matched with the existing models. This gives the designer full control over the passive modeling process, and again enables the ability to tradeoff runtime vs. accuracy.

An emerging capability for extremely sensitive blocks like VCOs allows the extraction of the full layout at the block level using full-wave 3D electromagnetic simulation. The performance of simulation tools like HFSS and computer platforms continues to improve and hence it is now possible to use 3D simulation on critical radio blocks. The advantage is that this rigorous method simulates all high-frequency layout effects including on-chip inductors, interconnect, coupling between on-chip passives and to other interconnect structures, and substrate coupling. No assumptions are made regarding parasitics or coupling. Of course the net-based RLC extractors have their place in the RFIC flow, but there is always designer input to manage which parasitic effects to include. It is not always clear which parasitic effects are most critical in the circuit context. Rigorous EM extraction of the entire block removes any doubt in the process.

Figure 10 depicts an HFSS™ simulation project for the layout of an entire VCO block. All active elements and MoM capacitors have been removed and their terminals were replaced with lumped ports. The HFSS project contains 142 ports and was solved on a dual processor PC in just over nine hours. Simulation required 2.15 GBytes of RAM. Although the simulation is lengthy, it is still reasonable to run overnight and the results for this case were well worth the effort. Figure 11 shows plots of the VCO negative resistance generator S11 magnitude (blue) and phase (red). S11 must be above the green dashed line (S11 > 0dB) in order for the device to oscillate. It is shown here that when extracted parasitics computed by full-block extraction are included the device no longer oscillates. Such a failure would not have been discovered until after tapeout, fabrication, and test. This level of layout extraction and verification can be very valuable to design organizations to ensure first silicon success.
The next critical step is to extract package parasitics and add those effects to the circuit simulations. At RF frequencies even the smallest amount of lead inductance can have a significant effect on circuit performance. Figure 12 contains images of an HFSS model for a quad flat no-lead (QFN) integrated circuit package. Simulations were performed to extract a full S-parameter matrix for all leads. From these simulations we can compute lead inductance for all conductors. Figure 13 depicts the schematic for the UWB radio receiver including the T/R switch, variable gain LNA, balun, I/Q demodulator, and baseband filtering/AGC. This circuit was used to examine the effects of package parasitics on circuit performance. Figure 14 is a plot of the small signal performance of the circuit shown in Figure 13 with and without ground and supply lead inductance. The blue trace is the baseline with no ground or supply inductance included. As can be seen from this plot, the S11 response looking into the LNA is less than 0dB across the frequency range and hence the circuit is stable. The red trace is a plot of S11 for the LNA including ground and supply package lead inductance for the T/R switch. Again, the circuit remains stable. The green trace is a plot of S11 looking into the LNA when ground and supply package lead inductance is included for the T/R switch and LNA. These results show that the ground inductance, common to the first and second stages of the LNA, cause the circuit to oscillate. In the same simulation it was observed that the small signal gain of the LNA decreased by ~15dB. Adjustments to the design of the various blocks were performed to stabilize the circuit. 

Figure 10. Critical VCO circuit layout geometry as simulated in HFSS.

Figure 11. Plots of VCO negative resistance generator S11 magnitude (blue) and phase (red). S11 must be above the green dashed line in order for the device to oscillate. (a) Before full-block layout extraction shows oscillation at 4.4 GHz. (b) After full-block layout shows that device no longer oscillates.
Figure 12. Quad flat no-lead (QFN) IC package model. (a) Model in HFSS. (b) Finite element mesh.

Figure 13. UWB receiver schematic including T/R switch, variable gain LNA, balun, I/Q demodulator, and baseband filtering/AGC.
Figure 14. Input return loss looking into the LNA of the circuit shown in Figure 13 with and without ground and supply lead inductance. Blue trace is the baseline with no ground or supply inductance included. Red trace includes ground and supply package lead inductance for the T/R switch. Green trace includes ground and supply package lead inductance for the T/R switch and LNA causing the circuit to become unstable.

The final step prior to tape-out or additional chip integration is to perform full-chip verification in a system (behavioral) test bench. The verification can include transistor-level circuits for multiple circuit blocks with incorporation of all extracted parasitics. The system should allow designers to select the particular level of abstraction for individual circuit blocks in order to make reasonable trades between accuracy and simulation run time. Figure 15 depicts a circuit schematic for full-chip verification of radio transceiver transistor-level circuits within a system test bench. MBOA bit and frame accurate time-domain waveforms are automatically linked to the input of the receiver circuit. Nexxim circuit simulation is performed on the full receive chain with all extracted parasitics included. Figure 16 contains plots of some representative results from the full-chip analysis. Figure 16 (a) is a spectral plot of the signal at the input to the receiver and Figure 16 (b) is a constellation plot showing the detected QPSK symbols at the receiver.

Figure 15. Full-chip verification for radio transceiver transistor-level circuit in system test bench.
APPLICATIONS

The RFIC design solution is applicable to many diverse applications from sophisticated analog-digital SoCs containing wireless front-ends to simpler RFIC devices that only contain RF circuit blocks. The method provides for higher fidelity in the simulation of the sensitive and critical analog sections by combining rigorous EM extraction with more powerful circuit simulators in an integrated design flow. Wireless and high-speed devices for networking and communications provide the greatest opportunity for this flow. A selection of likely applications is:

- Cellular CDMA power amplifier
- 10Gb/s Backplane Transceiver
- GHz-frequency PLL
- Gb/s Data Converter
- UWB Radio Transceiver.

UMC - ANSOFT COLLABORATION

UMC and Ansoft have a shared vision regarding partnerships and the need for advanced technology in the SoC design flow. Partnerships are developed to address significant needs in the IC design industry that align with the mission of both partners. The best partnerships are those that have the additional benefit of scaling the business of the members of the partnership and the business of their joint customers. The collaboration between UMC and Ansoft aims to build the most reliable solution for SoCs that contain high-performance analog front-ends by leveraging UMC’s advanced RFCMOS processes and Ansoft’s new technology for circuit and electromagnetic simulation.

UMC 0.13UM RFCMOS SOLUTION

UMC provides a logic-based technology platform with Mixed Signal/RF devices—a high performance, low cost solution for SOC designs. Besides providing a common technology platform, UMC also provides a design environment to support Mixed Signal/RF designs, meeting our customers’ time to market needs. The design environment includes Mixed Signal/RF foundry design kits, accurate models and P-cells, automatic schematic driven layout environments with links to electromagnetic extraction, simulation, and verification flow. The UMC 0.13um CMOS process offers low 1.2V core voltage, Ft of 105 GHz, Fmax = 90 GHz, and very low noise figure and high Q inductors.

Figure 16. Full-chip verification simulation results. (a) Spectrum at input to receiver. (b) Constellation plot of QPSK symbols detected at the receiver.
Ansoft provides electronic design automation (EDA) products that deliver high-performance and high-accuracy to support modern electronic and RF integrated circuit design. Ansoft’s best-in-class technology for circuit and electromagnetic simulation complements established monolithic IC design flows allowing designers to simulate sensitive analog circuits while including layout and packaging electromagnetic effects. Electromagnetic simulation using such tools as the High Frequency Structure Simulator (HFSS) provides accurate modeling of on-chip passives, layout, package parasitics, and substrate coupling. Ansoft’s Nexxim circuit simulator links directly into the mainstream Cadence design environment and adds high-performance transient and harmonic balance simulation. Harmonic balance, including the capacity to handle today’s larger designs, allows the engineer to predict non-linear performance of circuits including gain compression, IP3, inter-modulation, mixer spurious, phase noise, and sensitivity. Transient simulation plus Harmonic Balance in a singular simulator allows circuit validation in time- and frequency-domain under real-world communications waveforms.

The RFIC design flow significantly benefits fabless semiconductor design organizations now and in the future. Organizations large and small are highly concerned with achieving silicon success in order to avoid expensive re-spins and to hit a particular market window. The lifespan of wireless products is typically 12 – 18 months. Avoiding a program slip for re-spin can make the difference between successful design-in and missed opportunity. The RFIC flow provides a methodical approach to the design, simulation, and integration of complex SoCs. By allowing continuous monitoring of project development using system-level verification and co-design with transistor-level circuits, fabless design organizations can establish true metrics for design feasibility and efficacy. The examples shown here are for the UMC 0.13um RFCMOS process. The need for this flow increases as technologies scale to smaller technology nodes where parasitic and interconnect effects are more significant.

As technologies continue to scale to smaller technology nodes and include greater analog complexity and RF functionality, parasitic effects and the need to solve ever larger circuits faster, with more accuracy, becomes increasingly more significant. The adoption of newer methods is no longer a question of if, but when.
CONCLUSION

UMC provides a logic-based technology platform with Mixed Signal/RF devices—a high performance, low cost solution for SOC designs. Besides providing a common technology platform, UMC also provides a design environment to support Mixed Signal/RF designs, meeting our customers’ time to market needs. The design environment includes Mixed Signal/RF foundry design kits, accurate models and P-cells, automatic schematic driven layout environments with links to electromagnetic extraction, simulation, and verification flow. The UMC 0.13um CMOS process offers low 1.2V core voltage, Ft of 105 GHz, Fmax = 90 GHz, and very low noise figure and high Q inductors.
ABOUT THE COMPANIES

UMC
UMC (NYSE: UMC, TSE: 2303) is a leading global semiconductor foundry that manufactures advanced process ICs for applications spanning every major sector of the semiconductor industry. UMC delivers cutting-edge foundry technologies that enable sophisticated system-on-chip (SoC) designs, including volume-production, industry-leading 65nm, and mixed signal/RFCMOS. UMC’s 10 wafer manufacturing facilities include two advanced 300mm fabs; Fab 12A in Taiwan and Singapore-based Fab 12i are both in volume production for a variety of customer products. UMC employs approximately 12,000 people worldwide and has offices in Taiwan, Japan, Singapore, Europe, and the United States. UMC can be found on the web at http://www.umc.com.

ANSOFT CORPORATION
Ansoft is a leading developer of high-performance electronic design automation (EDA) software. Engineers use Ansoft’s software to design state-of-the-art electronic products, such as cellular phones, Internet-access devices, broadband networking components and systems, integrated circuits (ICs), printed circuit boards (PCBs), automotive electronic systems and power electronics. Ansoft markets its products worldwide through its own direct sales force and has comprehensive customer-support and training offices throughout North America, Asia and Europe. For more information, please visit www.ansoft.com.